

Interconnect fabrication processes and the development of low-cost wiring for CMOS products

by T. J. Licata
E. G. Colgan
J. M. E. Harper
S. E. Luce

As the cost and performance of integrated circuit (IC) interconnections, or "interconnects," become increasingly important to the development and manufacturing of successful advanced IC products, so also do underlying metallization and patterning processes. In particular, the goals of achieving product design specifications, low development cost (high and early yield), low manufacturing cost, and portability across products can only result from applying robust unit processes that combine to form integrable and scalable process modules. In this paper, we review the interconnect fabrication processes used to form currently manufactured IBM CMOS products, and describe the materials and process integration issues that motivated their selection. In addition, we identify factors which may inhibit application of the fabrication

processes to future products having smaller dimensions. The review suggests that large improvements in cost and scalability can be achieved by forming dual-damascene monolithic studs/wires. Previously, the dual-damascene approach was not generally applicable because of the lack of suitable metal deposition techniques for filling high-aspect-ratio features with highly conductive metal. However, recent advances may provide that capability both for near-term applications using Al-based wiring, and also for future applications using more extendible Cu-based wiring.

Introduction

As CMOS chips have become more complex, both on-chip interconnects and associated fabrication processes have become critical to the performance, reliability, and cost of integrated circuits. For example, the needs for higher

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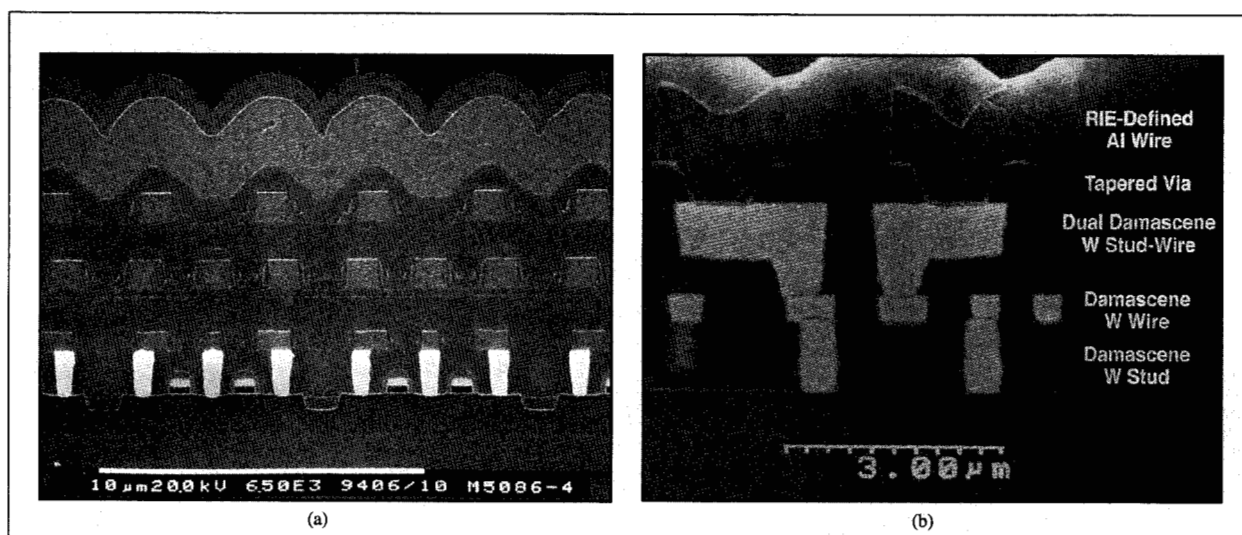


Figure 1

Cross-sectional SEMs of the wiring of (a) IBM PowerPC 603 chip and (b) IBM-Siemens 64Mb DRAM chip.

performance and lower cost per chip for successive CMOS generations have led to linear increases in the number of devices, but quadratic increases in the number of interconnects. These requirements have been met by increasing the number of interconnection or "wiring" levels, and by increasing the number of interconnects per level by reducing the wiring pitch. However, these tactics have made the signal propagation delay in the interconnects an appreciable and growing fraction of the total cycle time [1], and have increased the likelihood of failure due to electromigration and stress-induced void formation [2]. Furthermore, the fraction of product cost attributable to the wiring has increased dramatically, since the fabrication operations are sophisticated and are performed on capital-intensive tooling. Moreover, the scaling and reliability challenges require large development expenses.

In the past, dramatic increases in wiring density and reliability have been made possible by qualitative improvements in fabrication processes and integration. Similarly, future advances are expected to result from an understanding of the factors limiting the current processes, and from identification of applications in which blends of existing and emerging deposition and patterning processes can more efficiently produce the desired product. It is important to stress, though, that future progress must be accompanied by reductions in cost, since market forces continually decrease product price per unit of functionality.

Accordingly, in the first section of this paper, we review in detail the commonly used cloisonné and damascene wire

and stud fabrication processes. In particular, we examine the metal deposition and patterning unit processes, with an emphasis on how the processes must be adjusted to work together. Critical dependencies are identified which may hinder extensions of the processes to future products that require higher performance and lower cost. Next, we review dual-damascene processing, and describe how this comparatively simple process for forming monolithic studs/wires can provide superior performance and scalability for lower cost. Finally, since implementation of dual-damascene processing as a general interconnect solution depends upon the availability of manufacturable techniques for the filling of high-aspect-ratio features with highly conductive metal, we report on the status of several promising techniques for filling such features with Al or Cu alloys.

Currently practiced interconnect fabrication processes

• General

Current IBM integrated circuit products contain predominantly Ti/Al(Cu)/Ti/TiN wires patterned by reactive ion etching (RIE), and countersunk Ti/TiN/W studs patterned by chemical-mechanical polishing (CMP). These two approaches are analogous to the cloisonné and damascene techniques that have been applied for centuries to form inlaid metal features on jewelry. More specifically, in this paper, "cloisonné" refers to the patterning of a metal film followed by the deposition and planarization of an encapsulating insulating film, while "damascene" refers

to the patterning of the insulator, filling the recesses with a metal, and then removing the excess metal above the recesses. Note that in both cases, the final result is a planar interconnect process module that can be repeated as needed to form the desired number of stacked interconnects. Planarity is essential to the formation of successive fine-pitch interconnect levels, since lithographic definition of fine features is achieved using high-resolution steppers having small depths of field.

For example, **Figures 1(a) and 1(b)** show cross-sectional views of the PowerPC 603™ [3, 4] and 64Mb DRAM [5] wiring, respectively. The logic product utilizes highly conductive cloisonné Al wiring, since high-power signals must be routed relatively far across the chip. The DRAM, however, contains both cloisonné Al and damascene W wiring levels, since the primary requirements are low cost, high density, and high speed. Both products have damascene W studs where high density is required, and tapered vias for the less demanding connections to the final wiring level.

The various interconnect levels in both chips have been fabricated from the same set of technology elements. However, these elements have been combined and adjusted in different ways to provide interconnects optimized for the performance and cost requirements appropriate to each chip and level. By examining these elements and how they have been adjusted to work together, we can understand the limitations involved in extending them to future products.

• Currently practiced cloisonné metallization

Figure 2 shows a cross-sectional SEM of a typical Al-based wire of the PowerPC 603 chip. The wire is relatively thick and highly conductive, since its principal function is to carry high-current signals far across the chip. The cloisonné fabrication process for this wire is depicted schematically in **Figure 3**. It has been adopted because it utilizes well-developed unit processes that have proven to be manufacturable [6]. For instance, it is relatively inexpensive to deposit uniform blanket Al-alloy films using conventional physical vapor deposition (PVD). Furthermore, reactive ion etching (RIE) of Al-based films is well understood, and more scalable and easy to maintain in manufacturing than its wet-chemical predecessor, or "liftoff" [7]. Finally, RIE-defined wires having modest aspect ratios can easily be encapsulated using existing plasma-enhanced chemical-vapor-deposited (PECVD) oxides [8] and can be planarized by CMP.

However, experience has shown that these unit processes (and to a lesser extent the lithographic process) must be co-adjusted to widen the process window for manufacturing more aggressively scaled wires. For example, consider a generalized Al RIE process, where BCl_3 and/or Cl_2 source molecules provide energetic,

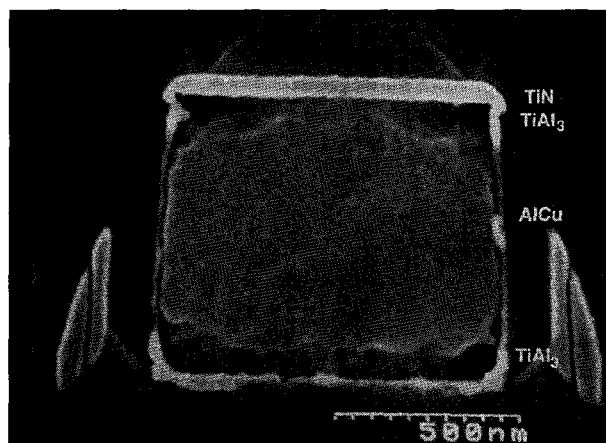


Figure 2

Cross-sectional SEM of Ti/Al(Cu)/Ti/TiN wire of the PowerPC 603 chip.

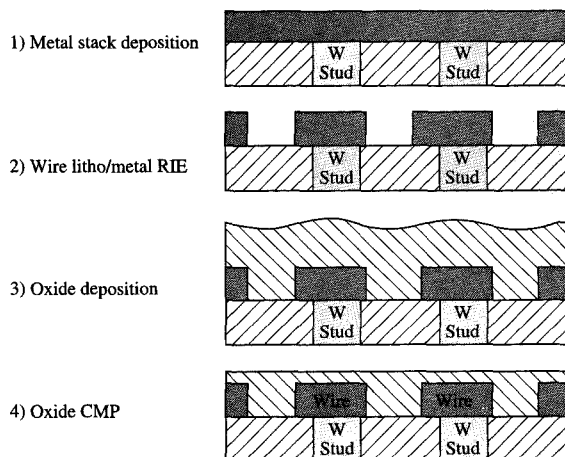


Figure 3

Process steps for forming cloisonné wiring.

directional Cl ions that react on the Al surface and form volatile AlCl_x compounds. In general, the chlorine system provides excellent Al/photoresist etching selectivity. Substrate bias is used to direct the ions and increase the etching rate, but impinging ions are then capable of sputtering photoresist atoms. Such sputtering is most effective at feature corners because of increased sputter yield at intermediate angles [9]. Unfortunately, the photoresist mask cannot be made arbitrarily thick, since

there is an upper limit to the photoresist thickness that can be applied and exposed uniformly. Hence, loss of mask integrity due to sputter erosion sets a limit on wire thickness and wire sidewall angle. Typical process parameters such as pressure, bias, and substrate temperature are then optimized to provide the best trade-off between feature profile and rate.

Similarly, different etching rates among features of different sizes or densities (microloading) also limit wire thickness and sidewall angle. As etching proceeds, wider features etch increasingly faster than narrower features because of their larger acceptance angles for reactive ions. Also, regions with much exposed metal (high pattern factor) etch more slowly than regions with little exposed metal (low pattern factor) because of limited etch-product diffusion. To ensure that all features have been properly isolated, over-etching of 20% or more beyond an AlCl optical emission endpoint can be utilized. Such over-etching worsens the above-mentioned mask erosion and recesses the underlying oxide etch stop because of the finite etch selectivity between Al and oxide. Areas with recessed oxide have higher aspect ratios that place greater demands on the subsequent oxide fill process. Thus, large wire thicknesses or wide ranges in pattern factor can lead to voids in the intralevel dielectric, and must be restricted accordingly.

The above integration limitations exist even with the best etch selectivities of Al to photoresist and oxide. In practice, though, these selectivities are decreased by the presence of alloying elements and impurities in the Al, and Ti-based films in the metal stack. Such additions to the metal stack are required for improved reliability and process integration, since a particular set of process and integration problems accompanies the use of Al, owing to its relatively low melting point and stable, passivating oxide.

To first order, the activation of many atomic and microstructural processes scales with homologous temperature (T/T_m). Specifically, since the melting temperature of Al is 933 K, a typical operation temperature of 358 K (85°C) corresponds to a T/T_m of ~ 0.4 . At this temperature, we expect significant atomic mobility through self-diffusion, resulting in mass transport, and the annealing of microstructural defects. Under such conditions, both electromigration and stress migration occur, and have been shown to be significant reliability detractors [10, 11]. Stress migration can also occur during the fabrication of multilevel Al-based wiring, and sets an upper limit on the thermal budget for its fabrication [12].

One way to enhance the reliability of an Al wire is to alter its microstructure. The term "microstructure" includes the often interdependent chemical and physical attributes of the film such as solute type and concentration, precipitate type and distribution, and grain

size, shape, and orientation. The manipulation is achieved through selection of alloying, process conditions, underlayers, and *ex situ* heat treatments. For instance, Al films deposited at 300°C or greater generally show enhanced resistance to electromigration and stress-induced migration because of their larger grain sizes (fewer grain boundaries) and more uniform (111) grain orientation distributions (preferred grain-boundary type) [13].

In addition, the incorporation of small amounts of Cu in Al films dramatically improves their resistance to electromigration failure [14] and has been widely adopted. This effect is significant but temporary, since the Cu atoms are themselves swept away over time by the "electron wind," leaving behind easily damaged, denuded Al. From this perspective, it is desirable to incorporate larger concentrations of Cu that can form θ -Al₂Cu precipitates, depending on interconnect dimensions and the details of associated heat treatments [15].

Unfortunately, the enhanced reliability afforded by Cu alloying is purchased at the cost of more difficult RIE patterning, and resulting limitations on θ -Al deposition temperature. Copper chloride reaction products are far less volatile than aluminum chlorides, and retard the etching. This is particularly problematic for Al₂Cu precipitates, which concentrate the Cu far above the average concentration. The conductive θ precipitates can leave residues that result in electrical shorting between adjacent wires [16]. This effect is minimized by striking a balance between reliability and processing windows. Typically, the Cu concentration is limited to 0.5 wt.%, and a low (e.g., 200°C) deposition temperature is used to ensure that the Cu cannot migrate sufficiently far to form large precipitates before patterning [17]. In addition, over-etching is used to remove alloy residues.

Note that the use of such low deposition temperatures limits the degree of underlying topography that can be covered, since improved Al step coverage results from the surface diffusion that occurs during higher-temperature deposition. It also adds process complexity, since heat treatments to increase the Al grain size must be carried out separately, after patterning. Alternatively, Cu can be kept in solution by depositing the Al at high temperature followed by rapid cooling [18]. However, this approach has been difficult to implement because of the higher concentrations of degassed chamber contaminants present during high-temperature deposition, and because of the difficulty in aligning photoresist patterns to alignment marks planarized by the more conformal Al.

The unintentional incorporation of impurities also makes RIE patterning of Al films more difficult. Like most metals, Al is very reactive and can incorporate significant amounts of oxygen during deposition. High levels of incorporated oxygen are routinely prevented, since they are easily detected through an increase in resistance of the deposited

films. However, smaller concentrations of oxygen that do not appreciably degrade film resistance have a considerable effect on film etchability. Eldridge et al. [19] have shown that the incubation phase of Al RIE, during which surface oxide is removed, can be lengthened by a factor of 3 or more for oxygen concentrations of 0.1–1.0 at.%. The plateau (Al removal) and terminal (feature isolation) etching phases are also significantly lengthened. Thus, to achieve low RIE times and reduce wiring fabrication costs, the Al deposition tooling and process must be optimized to achieve low base pressure and high deposition rate.

It is important to note that the relatively slow Al_2O_3 etching rate also limits the permissible degree of underlying topography. The slow Al_2O_3 etching rate promotes the formation of conductive residues or “stringers” near sidewalls, since the vertical thickness of the oxide to be removed by RIE increases with sidewall angle [20]. This effect could be minimized by producing less conformal coverage over steps through the use of an elevated deposition temperature, but the benefits in reducing stringer severity must be balanced against the difficulty in etching Al_2Cu precipitates and aligning patterns to marks covered with planarized metal.

Generally, other metallic films are included in the wiring stack in addition to the principal Al conductor, and are used to enhance the interconnect performance or the patterning process. Typically, all metal films in a stack are deposited in different chambers of an integrated PVD cluster tool to prevent exposure to air between film depositions. The cloisonné Al wiring of Figure 2 includes Ti-based films, since these can be deposited in elemental form, or reacted to form stable refractory compounds that are useful for a variety of purposes. It is highly desirable to utilize a material that performs several roles, since this reduces the number of deposition processes that must be optimized and supported in manufacturing. Moreover, a given product may already require PVD Ti to form a salicide cladding on diffusions for enhanced device contact [21]. It is important to note, however, that design specifications and process limitations restrict the height of a wire, so incorporation of supporting films comes with a resistance penalty because of displaced Al.

Specifically, the “Ti-over-and-under” wiring of Figure 2 uses elemental Ti as a base adhesion layer that also decreases contact resistance to underlying conductors by reducing interfacial oxides. This Ti underlayer, and the Ti overlayer deposited after the Al, are reacted by thermal treatment after patterning to form TiAl_3 , a moderately conductive, refractory intermetallic that is stable against electromigration and provides mechanical stability useful in resisting stress migration [22, 23] and hillock formation. Finally, a reactively sputtered TiN film is used as a cap layer to facilitate photolithographic definition of fine features by reducing the reflectivity of the stack.

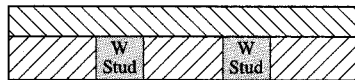
Fortunately, such Ti-based films etch well in the Cl_2 systems used to etch Al. However, the use of a Ti/TiN cap on Al in conjunction with photolithographic patterning can also limit the Al deposition temperature [24]. Since TiN is reactively sputtered with energetic bombardment, the deposited film has a highly compressive stress state. On the other hand, the Al is deposited at a high homologous temperature and is in tension after cooling to room temperature. Since the Al is constrained from relaxing by the Ti and TiN layers, the stress can be relieved by “grain collapse” if the Al grains are sufficiently large [25]. The resulting surface is very rough, and contains small holes in the Ti/TiN cap layer. During the lithographic process, trimethylammonium hydroxide (TMAH)-based developers etch the Al below the holes. The walls of the Al cavities are oxidized during the rinse, producing round Al_2O_3 micromasks that leave ring-shaped residues (“ring defects”) in field areas after the RIE patterning. A thicker Ti/TiN cap is less likely to form holes, but this approach scales poorly because of constraints on allowable wire resistance and capacitance. The problem can also be solved by utilizing developers that do not etch Al [26], but such developers bring a different set of difficult problems. Thus, for TMAH-based developers, the problem is minimized by retarding Al grain growth by using a lower deposition temperature. As mentioned above, however, this is disadvantageous with regard to Al reliability, since it produces more grain boundaries which act as short-circuit paths for migrating atoms.

• *Currently practiced damascene metallization*

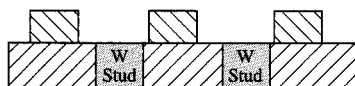
Damascene processing is an alternative method for fabricating planar interconnects [7, 27]. As shown in Figure 4, damascene wires (or studs) are formed by depositing a dielectric layer on a planar surface, patterning it using photolithography and oxide RIE, then filling the recesses with metal. The metal in the field is removed by CMP, while the troughs remain filled with metal. For example, Figure 5 shows a cross-sectional SEM of a damascene wire similar to the bit lines of the 64Mb DRAM of Figure 1(b). The process is nearly identical to that used to form the W studs in the logic and DRAM products of Figures 1(a) and 1(b). In both examples, sputtered Ti/TiN liners have been coated with CVD W metal, then polished back to oxide.

The damascene approach has been adopted for these applications, since it efficiently provides the high yield and large process windows required for volume manufacturing. The use of CMP leads to a decrease in the number of interlevel shorts and lowers defect densities, since unwanted surface material is easily removed. Simultaneously, upon completion of CMP, the wafer surface is returned to the globally planar state, extending process windows for subsequent lithographic, etching, and CMP processing steps. Furthermore, the choice of

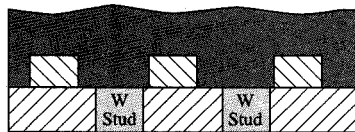
1) Oxide deposition



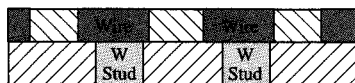
2) Wire litho/oxide RIE



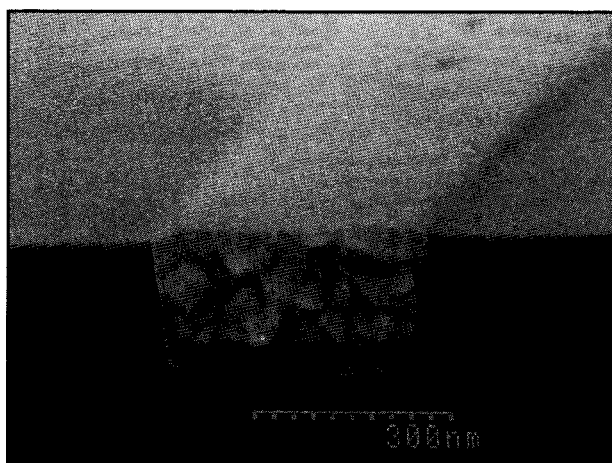
3) Metal stack deposition



4) Metal CMP

**Figure 4**

Process steps for forming damascene wiring.

**Figure 5**

Cross-sectional SEM of damascene Ti/TiN/W wire.

embedding metal in a previously deposited insulator is advantageous because mask alignment, dimensional control, rework, and the etching process are all easier when applied to dielectric rather than metal films. Damascene processing achieves these benefits, however, by shifting the enhanced filling and planarization requirements from dielectric to metal films, and by shifting control over interconnect thickness from metal deposition to insulator patterning and metal CMP.

As mentioned above, sputter deposition has emerged as the preferred metal deposition technique because it can be used to deposit many conductive materials, at high deposition rates, with good uniformity and low cost of ownership. However, conventional sputtering does not fill or coat recessed features well, and thus is poorly suited to damascene processing. Sputtered atoms are typically ejected from a target in all directions, though the degree of flux directionality depends on the specific material being deposited, and on deposition conditions [28]. Atoms are then deflected by collisions with Ar atoms between the target and substrate. This poorly oriented sputtered flux results in recessed surfaces to accrete atoms at a lower rate than the top surface. The discrepancy worsens for deeper, narrower (high-aspect-ratio) features. In addition, fill is especially bad for corners of recesses, which have relatively small acceptance angles for flux, and for thick depositions, since the upper surface deposition can block incoming flux and produce a void in the recessed feature [Figure 6(a)].

The filling afforded by sputter deposition has been significantly improved by collimating the sputtered flux [29–32]. As shown in Figure 6(b), collimated flux is produced by removing sputtered flux that approaches the substrate at a large angle from the surface normal. Typically, this is achieved by inserting between the target and substrate a collimator plate having an array of hexagonal cells. Flux traveling at a large angle deposits on the cell walls, while flux at a smaller angle is transmitted to the substrate. Rerandomization of flux by collisions is minimized by sputtering at low Ar pressure, thus increasing the mean free path of the sputtered material, and by restricting the separation between the target and substrate.

Plate collimation has been successfully implemented in currently manufactured products having aspect ratios up to 3.0. However, collimator clogging problems discourage its application to future products having significantly higher aspect ratios. For instance, plate collimation decreases deposition rate in proportion to the aspect ratio of the collimator used. In a typical process, a collimator having hexagonal holes 1 cm wide and 1.5 cm thick (1.5 aspect ratio) is inserted midway in the 9-cm space between the cathode and wafer. A sputtering pressure of 1 mT is used, which corresponds to a mean free path of 5 cm, significantly larger than the 3.5-cm plate-to-substrate spacing. Under these conditions, the initial deposition rate is reduced by a factor of 3 from the uncollimated rate (thus increasing product cost), but the close-coupled conditions produce good center-to-edge deposit uniformity. However, as wafers are processed, a deposit develops on the upper surface of the collimator that extends laterally over the holes and blocks progressively more flux. As the collimator deposit builds, the aspect ratio of the collimator increases, thereby changing the ratio of recessed surface to

top surface coverage ("fill factor"). The deposition time can be continually adjusted over the life of the collimator to ensure consistency of surface thickness, but the changing fill factor can influence interconnect performance and the CMP process, and is less easily remedied. Eventually, the collimator plate must be replaced, typically when the deposition rate has fallen to half its original value. This produces tool down-time that also increases product cost. These problems are exacerbated by the need for higher-aspect-ratio collimators in order to fill or coat higher-aspect-ratio features.

For these reasons, collimated sputtering is acceptable for thin liner depositions to cover features having moderate aspect ratios, but is not an appropriate technique for the complete filling of such features. Instead, for short-distance wiring such as studs and DRAM bit lines for which the high conductivity of Al is not required, chemical-vapor-deposited (CVD) W has proven to be a robust process that integrates easily with liner deposition and CMP to provide a manufacturable interconnect module. CVD W relies on the transport of gaseous reactants to the wafer surface and surface diffusion to produce films that conform to underlying topography. The most widely applied process deposits blanket W films from SiH_4 and H_2 reduction of WF_6 in a cold-wall reactor. The process is attractive, since highly conductive films are produced at $\sim 0.25\text{-}\mu\text{m}/\text{m}$ deposition rates using moderate temperatures of $350\text{--}400^\circ\text{C}$. The W films have a resistivity of $\sim 13\text{ }\mu\Omega\text{-cm}$ for 100-nm -scale films, while that of thicker films approaches $10\text{ }\mu\Omega\text{-cm}$. (The resistivity of bulk W is $5.65\text{ }\mu\Omega\text{-cm}$.) Moreover, the W is easily patterned using CMP since it is hard and corrosion-resistant. It is also compatible with RIE formation of overlying Al-based wires, since it offers excellent etch selectivity in the preferred Cl-based chemistries.

CVD W requires the use of underlying conductive barrier and "seed" layers to prevent consumption of substrate Si from reaction with WF_6 at the contact level, and to promote distributed nucleation and low contact resistance. Again, Ti is desirable, since it provides good adhesion and low contact resistance and is readily available. However, it is not sufficient, because the F from the WF_6 reacts with the Ti and produces a brittle, high-resistivity compound that worsens adhesion and contact resistance. Fortunately, inserting a TiN film between the Ti and W solves these problems by enhancing W nucleation while preventing the reaction of F with the Ti or any exposed Si [33]. A W seed layer is then formed on the TiN by SiH_4 reduction of WF_6 . The SiH_4 -to- WF_6 ratio is critical to process optimization, since insufficient SiH_4 concentrations lead to excess F and degradation of the TiN, while excess SiH_4 produces high-resistance films having poor conformality. Finally, the majority of the deposition is performed by means of H_2 reduction of WF_6 ,

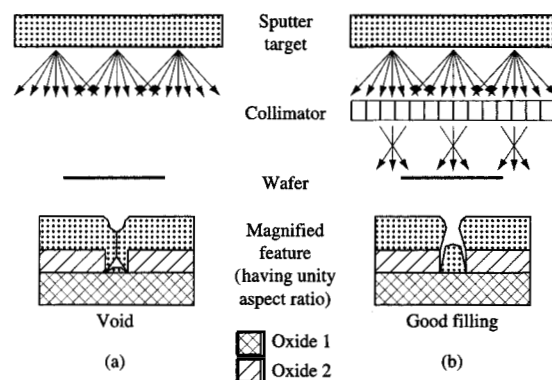


Figure 6

Schematic depiction of (a) conventional and (b) collimated sputter deposition, and associated filling of feature.

because that process produces a W film that has lower resistivity and better conformality.

Since Ti-based liners are less conductive and less easily polished than W, it is desirable to keep them as thin as possible in current products, and scale the thicknesses down for future products. However, since the PVD liners are not conformal, inadequate coverage of recesses or foreign material defects can allow F to react with the underlying Ti, causing the liners to detach from their substrate [34, 35]. The TiN layer breaks and curls up, since the film is in tension. The CVD-W then deposits on the rolled-up TiN, forming a "mound" or "mushroom" of W. Unfortunately, this is most likely to happen at a stud opening, where detracton from yield results (defects in field areas are polished away). Recently, the prospects for better liner coverage have improved, since CVD TiN [36–38] and Ti [39] processes have been developed and offered by process equipment vendors. In general, CVD Ti and TiN offer good conformality, but require higher deposition temperatures and contain higher levels of impurities than do PVD films. If these processes prove to be manufacturable, CVD liners will facilitate the use of CVD W at $0.25\text{-}\mu\text{m}$ design rules.

After deposition, CMP is applied to complete the inlaid structure. In the CMP process, material is removed from the wafer through the combined effects of a polish pad and an abrasive slurry [40]. Typically, chemical dissolution of material is aided by a mechanical component which is useful in removing passivating surface layers. Chemical and mechanical selectivities between materials are desired, since CMP must remove the metal overburden without removing appreciable amounts of inlaid metal or reducing interconnect thickness.

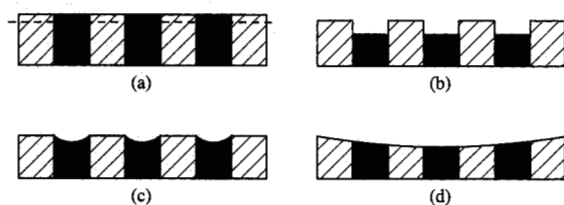


Figure 7

Schematic depiction of polished features: (a) ideal, (b) etched, (c) dished, and (d) eroded. Black: metal; hatched: oxide.

Figure 7 shows schematic cross sections of (a) desirable and (b–d) undesirable polishing results. Figure 7(a) depicts the ideal polished feature, where planarity has been achieved by removing all overlying metal without removing any oxide. This outcome would result from using a process that displays extremely high CMP selectivity between metal and oxide films, and negligible chemical etch rates for both materials. In practice, finite selectivities are obtained, and the best possible profile is thinned slightly, as indicated by the dotted line. In contrast, Figure 7(b) shows an undesirable profile: The oxide has been preserved, but the metal has been uniformly recessed. Such a profile results from an overly aggressive chemical system that removes metal in the absence of the mechanical polishing component. Similarly, Figure 7(c) shows a badly dished profile: The oxide has remained intact, but the metal has been preferentially removed from the center of the feature. This outcome is most severe in wide features if a softer polishing pad is used, and is exacerbated by the use of polish-resistant liners that slow the polishing rate in the final stage, when the overburden has been removed but the features are not yet fully isolated. Finally, Figure 7(d) shows a profile for which both metal and oxide have been thinned in a nonuniform fashion that depends on pattern density. This outcome results from insufficient selectivity between the metal and oxide and is also worsened by the use of polish-resistant metal liners. In practice, this effect is always present to some degree, and is taken into account by restricting the pattern factor of the wiring design. Further, the oxide deposition, oxide etch, and metal deposition processes are adjusted to provide a deeper inlaid metal feature which yields the correct interconnect thickness after CMP.

Scratching of the polished surface must also be avoided. Scratches in the inlaid metal can reduce the cross section locally, resulting in an elevated current density and/or elevated stress, thereby accelerating interconnect failures.

Moreover, scratches in the oxide surface can decrease yield. If a scratch breaks the oxide boundary between metal wires, metal can smear or deposit in the channel of the scratch, leaving shorts which are impossible to correct without thinning or recessing the wires. However, scratches in oxide field areas can induce shorting in succeeding damascene metal levels, since a conformal oxide deposition will replicate the recess in the next dielectric layer. Deposited metal will fill the scratch and be difficult to remove unless the slurry contains a strong chemical component likely to recess the wire. Scratching of all materials is minimized by using a slurry that resists agglomeration of the abrasive particles or polish by-products, and by using softer pads that provide slow polishing rates. However, metal scratches can also be avoided by limiting the application of CMP to relatively hard metals that resist scratching, and by limiting the size of the features to be polished. The latter tactic is effective, since scratching particles are unlikely to penetrate deeply into metal features that are fragmented by harder oxide regions.

It is important to note that in addition to maintaining feature profile and minimizing scratching, CMP processes must be optimized for high rate, uniformity, reproducibility, and manufacturability [41]. Accordingly, CMP processes tend to be tuned to a specific application and are not quickly extendible to novel situations. However, once optimized, CMP provides low-cost fabrication that is robust against variations in other processes.

As shown by comparing Figures 3 and 4, the damascene and cloisonné processes require approximately the same number of steps to produce a planar interconnect level. In principle, the cost of damascene processing should be lower because its constituent unit processes are less interdependent, leading to wider process windows that facilitate high product yield in both the development and manufacturing phases. However, damascene processing provides further reductions in process cost by allowing consolidation of stud and wire fabrication processes. In the dual-damascene process, a monolithic stud/wire structure is formed from the repeated patterning of a single thick oxide film followed by metal filling and CMP (**Figure 8**). First, a relatively thick oxide layer is deposited on a planar surface. The oxide thickness is slightly larger than the desired final thicknesses of the stud and wire, since a small amount of oxide is removed during CMP. Stud recesses are formed in the oxide using photolithography and RIE that either partially drills through the oxide or traverses the oxide and stops on the underlying metal to be contacted. The wire recesses are then formed using a separate photolithography step and a timed oxide etching step. If the former stud RIE option is used, the wire etching completes the drilling of the stud holes.

Alternatively, the wire recesses can be formed first, but this approach makes the photolithography for the studs more difficult, since the resulting surface is less planar. Next, the stud/wire metallization is deposited, then planarized using CMP. The resulting interconnects are significantly less expensive to fabricate than the more conventional cloisonné wires on damascene studs, since one oxide deposition, one metal deposition, and one oxide CMP planarization step have been avoided. In addition, contact resistance between the wire and underlying stud is removed as a source of process variation, since no interface exists within the resulting monolithic structure.

This approach has been successfully applied in manufacturing of the IBM 4Mb DRAM chip [42] and has been qualified for manufacturing of the IBM-Siemens 64Mb DRAM chip shown in Figure 1(b) [5]. For both, PVD Ti/TiN films were used as liners, while CVD W formed the principal conductors. The previously developed W CMP process was employed for planarization. Superior product yields were attained, and capital spending for manufacturing tooling was ~14% below the level required for the alternative damascene-stud/cloisonné-wire fabrication process.

Note, however, that the dual-damascene process exacerbates the fill and planarization challenges already described for single-damascene processing. Specifically, the metal films must now fill features having aspect ratios much greater than 1. This is easily attained with CVD W, provided the adhesive liner film continuously covers the recessed surfaces. To obtain adequate coverage using collimated PVD Ti/TiN liners, a larger thickness must be applied which is difficult to polish away without dishing the more easily removed W. Moreover, the conformal filling afforded by CVD W results in local recesses over the high-aspect-ratio dual-damascene features that contribute to dishing during polishing.

The W dual-damascene process for forming lines and studs has restricted applicability and extendibility, since most wiring applications require the use of more highly conductive Al-based lines. An alternative metallization for the IBM-Siemens 64Mb DRAM chip combined mostly standard unit processes to extend the dual-damascene structure to produce more conductive interconnects. Specifically, the Ti/TiN/W film stack mentioned above was replaced by a Ti/AlCuSi/TiN/W stack [43]. Collimated sputtering was used to enhance filling by the Ti, AlCuSi, and TiN films. CVD W completed filling of the structure and left a polishable cap necessary in the absence of a manufacturable Al CMP process. The film thicknesses and deposition temperatures were chosen to ensure that the void resulting from the nonconformal AlCuSi filling occurred near the top of the wiring troughs and was polished away to leave a void-free structure. Also, AlCuSi coverage of the upper sidewalls was deterred through

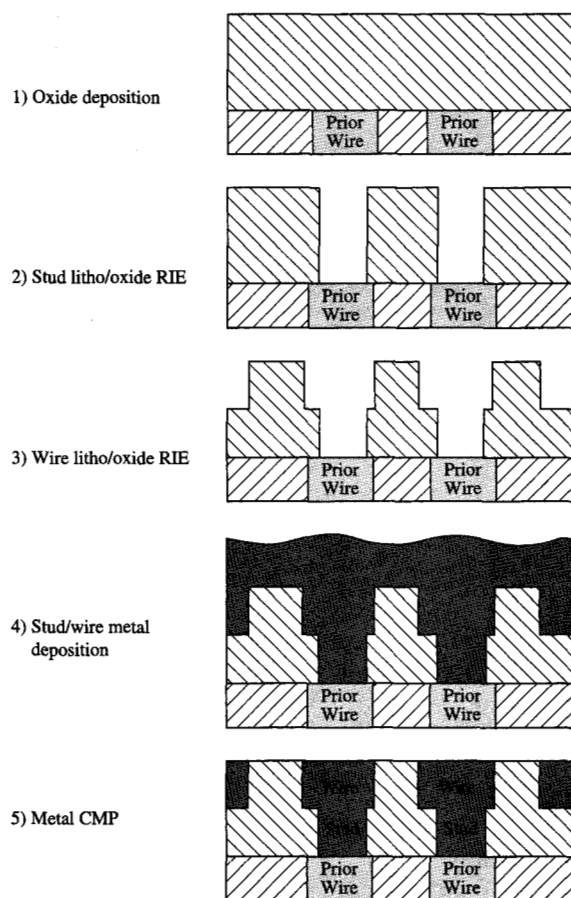


Figure 8

Process steps for forming dual-damascene wiring.

choice of alloying and deposition temperature, since exposed AlCuSi "rails" corrode if exposed to the W slurry in the final stages of CMP.

However, the W-capped technique must be viewed as an interim solution. The conductivity improvement is modest, and is purchased at the cost of process complexity and added interfaces in the combination PVD/CVD metallization. In addition, the need for a W cap introduces severe design rule restrictions. Features may not be so wide that CMP dishing penetrates the cap, since the W slurry corrodes exposed AlCuSi. Electrical shorts can result from smeared AlCuSi on circuit features, or from scratches caused by hard W fragments that detach from the broken cap. Alternatively, the cap can be thickened, but this increases the interconnect sheet resistance by displacing AlCuSi from the structure, or increases the aspect ratio for AlCuSi filling, thereby decreasing filling

efficiency and manufacturability. Clearly, more efficient and extendible solutions are needed.

Dual-damascene interconnects and enabling metal deposition processes

• General

Much of the technology described above has been used for many years for high-yield manufacturing of a variety of micron- and submicron-scale products, and is clearly successful. However, we expect that the cost and scaling issues identified above will become critical for the manufacturing of sub-0.35- μm -scale products. For the cloisonné technique, many process steps are required to yield the planar interconnect structure necessary for high-yield, fine-pitch, multilevel metallization. In addition, unit process problems include the difficulty in aligning a photoresist pattern on Al-alloy films, the difficulty in etching Al_2O_3 , the difficulty in etching Al_2Cu precipitates, and the restrictions on film microstructure necessary to address these problems. Moreover, RIE patterning is not easily implemented for the Cu-based wiring required for future products. The damascene technique addresses the cost issue by facilitating yield and requiring significantly fewer process steps. However, enhanced unit processes are required to provide wide process windows and scalability.

Over the past few years, novel metal deposition techniques have been developed which enable dual-damascene processing. Some are useful for Al-based filling and allow rapid implementation of dual-damascene wiring. Others are applicable to a variety of metals and should facilitate scaling of the damascene technology to future products.

• Enhanced physical vapor deposition techniques

For many years it has been recognized that the relatively low melting point of Al (660°C) allows atoms to diffuse rapidly along surfaces and through grain boundaries at commonly employed processing temperatures (300–500°C). This has been seen as a disadvantage, since exposing previously formed interconnects to high temperature can promote the formation of stress-induced voids that detract from interconnect reliability. Some workers, however, have attempted to use high temperatures in conjunction with standard PVD to enhance Al filling and improve overburden planarity. While early efforts yielded intriguing results on a laboratory scale [44, 45], commercially available process equipment lacked the cleanliness and wafer temperature uniformity needed for adequate product process window.

More recently, having obtained years of experience with PVD modules operating at conventional temperatures, commercial equipment manufacturers have developed PVD Al chambers for clustered manufacturing tools that routinely provide the conditions necessary for effectively

utilizing Al diffusion as a process parameter [46–48]. This capability has been achieved through enhanced hardware and rigorous maintenance procedures. For example, to reduce the level of contaminants during processing, such modules are typically baked for several hours at about 150°C prior to use (limited by the O-ring seals). Such bakeouts facilitate the rapid desorption and removal of water and gases that adsorb on the inner surfaces when the module is vented for a target change or maintenance. Unfortunately, complete removal of the adsorbed gases would require the use of higher temperatures and longer times that are incompatible with low-cost manufacturing. Instead, outgassing is reduced during operation by flowing cold water through the module walls. This is necessary, since infrared radiation from a 550°C heater table heats the module and increases the desorption of contaminants that remain after the bakeout. In addition, point-of-use filtering of Ar working gas, larger cryopumps, and larger flow rates are used to improve the purity of the ambient. Finally, since Al diffusion is a strong function of temperature, wafer temperature must be uniform and repeatable. Several manufacturers have released products that operate at 550°C with <2%, 1σ uniformity.

There are several processes for filling features with Al-based films that utilize such an approach, referred to generally as the “hot-Al” approach. The particular processes chosen depend on the aspect ratios and shapes of the features to be filled, the degree of overburden planarity desired, whether previous or later wiring levels consist of conventional or hot Al, and the raw process time (wafer throughput) required for cost-effective manufacturing. In all cases, the wafer is first heated to 350°C or more in a degassing chamber to drive off moisture and other volatile contaminants. Then a thin Ti film is deposited to reduce contact resistance to the underlying conductor and inhibit Al agglomeration. A TiN barrier layer can be added to prevent the TiAl_3 reaction, and is required to prevent spiking when the hot Al is used to contact Si. In the simplest variation, an Al alloy is slowly sputtered onto the adhesive or diffusion barrier layer. Features having aspect ratios <1 can be effectively filled though Al surface diffusion in this manner at temperatures of 450°C and higher. For features having aspect ratios of about 1.5, a two-step deposition/reflow process can be used. The PVD Al-alloy layer is deposited without collimation, using a conventional module at a conventional processing temperature. The wafer is then transferred under vacuum to a second module having a heater table maintained at about 550°C, where the deposited film flows into the underlying recesses through a bulk diffusion mechanism. Finally, for very aggressive aspect ratios of 2 or more, a two-step cold/hot PVD process is practiced. In this process, deposition of collimated PVD Ti-based liners is followed by deposition of a thin layer of collimated

"cold" PVD Al alloy. It is particularly important for robust filling that the liner layers form a continuous film over the surface of the features to be filled. The wafer is then transferred under vacuum to a second PVD Al-alloy module with a heater table maintained at 475–550°C, where the Al alloy is deposited slowly enough to fill features through enhanced surface diffusion. The various film thicknesses, deposition rates, and process temperatures used are optimized to avoid Al agglomeration, since this is a principal process window limiter, and to establish overburden planarity if desired.

Such a hot-Al process has been applied in conjunction with a novel CMP process to produce a dual-damascene stud/wire structure for the IBM–Siemens–Toshiba 256Mb DRAM chip [49]. **Figure 9** shows a cross-sectional SEM of its three-level metallization structure. As for several previous products, the first metallization level (bit-line level) is damascene W, while the third metallization level is a conventional RIE-defined Al-based stack. However, the second metallization level and underlying stud level are monolithic Al alloy fabricated at 0.25- μ m design rules. Filling of the high-aspect-ratio stud/wire features is attained using a cold/hot process similar to that described above. Planarization is achieved using a novel CMP process having slurry and pad optimized for the unique properties of Al.

In this example, adjustment of the accompanying lithographic and etch processes enhances the filling and planarization process windows. After the contact holes have been etched, but prior to forming the wiring troughs, an organic antireflective coating (ARC) is applied which facilitates the subsequent use of deep-UV lithography. The ARC spontaneously tapers at the edge of the contact holes. Photoresist to define the wiring troughs is applied, exposed, and developed. Then oxide RIE forms the troughs and transfers the tapered ARC profile to the edges of the walls of the vias only where wire and via shapes overlap. Such self-aligned tapering reduces the feature aspect ratio without increasing via area in an undesirable fashion, and thus enhances PVD film coverage without violating design rules or adding process complexity. Accordingly, robust filling can be achieved at a lower processing temperature, or using thinner films that are more quickly removed by CMP.

Interconnects fabricated using this process showed unusually good resistance to electromigration failure [49]. Specifically, typical stress conditions of 1×10^6 A/cm² at 250°C produced relatively few failures compared to conventionally fabricated interconnects. The improved stability of the dual-damascene hot-Al interconnects resulted mainly from the optimized microstructure. Specifically, the high-temperature process produced a mean Al grain size of approximately 2 μ m, so there were few grain boundaries in the 0.25- μ m-wide wires. Thus,

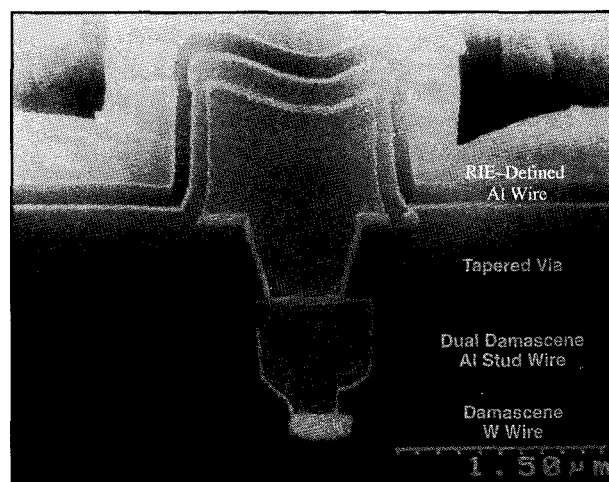


Figure 9

Cross-sectional SEM of three-level metallization structure (including dual-damascene hot-Al stud/wire) of the IBM–Siemens–Toshiba 256Mb DRAM chip.

atoms must migrate by slower interfacial or lattice diffusion, rather than by more rapid grain-boundary diffusion. In addition, X-ray diffraction measurements show that the Al grains are very well aligned along the (111) direction, so few of the grain boundaries are highly disordered.

Note that additional improvements in reliability may be obtainable through selection of Al alloying, since, to first order, the damascene approach removes restrictions on the types and amounts of alloying that can be used. Accordingly, novel Al-based metallizations can be designed, evaluated, and implemented without regard to the volatilities of solute–halogen complexes [50].

For several reasons, the advanced DRAM application is the logical point of entry for the hot-Al/CMP dual-damascene structure. Owing to the nature of the DRAM product life cycle, low manufacturing cost is of paramount importance. As mentioned previously, interconnect formation using the dual-damascene process requires relatively few process steps, while CMP provides for narrow linewidths, the easiest path to high, early yield, and robust process windows. Furthermore, by applying the process only once on the chip, and by having an underlying W bit line, any difficulties that might result from the effects of high temperatures on preexisting Al interconnects are avoided. The fact that the overlying metal level is of significantly larger pitch is also fortunate, since this decreases the degree of planarity required from the Al CMP process. The hot-Al process, *per se*, is attractive since it is evolutionary from the Ti-based liners and Al-alloy films used in existing interconnects, and can

thus benefit from the large integration, reliability, and manufacturing databases associated with these materials. It is noteworthy that the process can easily be implemented in existing manufacturing lines, since only modest modifications are required to existing PVD cluster tools.

It is also possible to realize cost savings over current interconnect fabrication processes by utilizing hot-Al or some other planarizing deposition technique with cloisonné patterning. This technique, referred to as Simultaneous Planar Repeatable INTERconnects, or SPRINT [51], forms monolithic stud/wire interconnects by filling a contact hole with metal and RIE patterning the planar overburden to form wiring. SPRINT provides some of the benefits afforded by dual-damascene processing. One metal deposition and one planarization step are eliminated, and a reliable monolithic stud/wire structure is formed. However, overburden planarity is very important, and must be achieved without manipulating overburden thickness, since this is set by the wiring sheet resistance specifications. Further, photoresist alignment on the planar Al is problematic, and most likely requires application of a "blockout" mask and RIE step to remove Al from the alignment marks. These additional steps detract from the cost advantage gained by simultaneous stud/wire formation. Finally, design rule restrictions or additional process steps are required for application to fine-pitch metallization, since the RIE used to define the wires can also etch uncovered underlying Al in the studs.

The enhanced filling provided by hot-Al deposition results from the higher surface mobility and diffusion of Al atoms at high homologous temperatures. However, it is generally desirable to decouple feature filling from process temperature, since this gives the process engineer the maximum flexibility in designing interconnect microstructure and minimizes the impact of temperature on preexisting structures. Further, a filling technique based on a high homologous temperature cannot be applied to Cu because temperatures near the melting point of Cu (1073°C) are incompatible with conventional IC processing. Filling techniques for Cu are needed, since Cu should provide scaling advantages required for future products [52, 53]. For instance, the resistivity of bulk Cu ($1.68 \mu\Omega\text{-cm}$) is significantly lower than that of bulk Al ($2.66 \mu\Omega\text{-cm}$). Thus, more current can be carried by a Cu wire of given dimensions, or dimensions (and hence capacitance) can be reduced for a given current. Moreover, because of its higher melting point, Cu resists electromigration better than Al, so that, other factors being equal, less alloying is required and less elevation of the intrinsic resistivity occurs.

As mentioned previously, one way to improve feature filling independent of wafer temperature is to improve the directionality of the sputtered flux through collimation, but this technique has drawbacks that limit its application in manufacturing. Fortunately, directional flux can also be

obtained by ionizing the sputtered material and biasing the wafer. For many years, biasing has been used in conventional sputtering processes to accelerate sputtering gas ions toward the substrate. Such bombardment can modify the microstructure of a growing film, or resputter deposited material preferentially at corners to improve the step coverage. In practice, features having aspect ratios of 1 or less can be filled in this manner. Ionization of the depositing metal flux provides additional improvements in feature filling because the ionized metal flux is rendered very directional by acceleration across the thin, flat discharge sheath. Also, the energetic metal ions are very effective at sputtering away the overhanging metal at step corners. Unlike plate collimation, this technique does not suffer from low deposition rate or inconstancy of fill factor.

One embodiment of the technique is partially ionized beam deposition, in which an evaporation source is equipped with an electron bombardment ionization region to ionize some fraction (usually several percent) of the depositing flux. Features having aspect ratios up to 2.0 have been successfully filled in this manner with Al at 210°C [54]. Partial planarization was noted at 320°C. However, evaporation sources are not practical for depositions on 200-mm-diameter wafers because of the prohibitively large throw distances and vacuum chambers required for good uniformity on batched wafers. Fortunately, ionized metal flux can also be achieved using standard PVD sources and ionization of the sputtered flux by a second plasma [55–57]. Ionization fractions of 75% or more are provided by a dense plasma excited using either microwaves at the ECR frequency of 2.45 GHz, or inductively coupled RF. A low-voltage bias (about 20–40 V) on the substrate holder directs the ionized metal flux at normal incidence to the wafer and imparts enough energy to resputter metal from feature edges.

This technique has produced conformal coverage of Ti and TiN liner films, and complete filling of AlCu and Cu on features having an aspect ratio of 3 at temperatures below 100°C. In the latter case, the resputtering effect introduces residual topography above the filled features that may complicate planarization, but this can be ameliorated by employing higher processing temperatures or a multistep deposition having a tailored bias in its final stage. It is important to stress that ionized PVD has several attractive advantages. Unlike plate collimation, the deposition rate is not lower than that obtained for uncollimated films. Further, since there is no collimator plate to clog, scalability is straightforward, the deposition rate and fill factor remain constant over time, and downtime for collimator plate changes is avoided. Finally, the enhanced filling is evolutionary from existing PVD processing, and hence retrofittable to existing tooling and more easily extendible to new wiring materials.

• Chemical vapor deposition

In CVD, an ambient conveys to the substrate a complex containing the species to be deposited. A surface reaction deposits the metal, and by-products diffuse away from the surface. In principle, it should be possible to deposit truly conformal films in that manner, since the metal atoms are delivered to the substrate without the preferred directions or high translational energies characteristic of PVD techniques. However, since film nucleation events are statistical in nature, it is critically important to maintain precise control of substrate cleanliness, process parameters such as temperature, and ambient composition and purity. Furthermore, the details of mass transport of reactants and products that lead to CVD conformality are complex and dependent on both chemical and ballistic effects [58–60]. Accordingly, CVD cannot be quickly adapted to a wide variety of metals. In the case of Al or Cu, additional complexity arises from the need to alloy with various solutes for resistance to electromigration, stress migration, and corrosion.

In its most basic form, blanket (nonselective) CVD coats the entire substrate surface with metal. As mentioned above, blanket CVD W processes are routinely applied in manufacturing, and recently developed CVD TiN and Ti processes look promising. Selective CVD W has also been developed and is being used to manufacture the Toshiba® 16Mb DRAM [61]. Selective deposition can provide integration leverage by eliminating the need for sputtered seed layers or by reducing planarization requirements. Much progress has also been made in the past few years on CVD Al and Cu, though these latter processes have not yet been applied in manufacturing.

For instance, a prototype manufacturing cluster tool has been constructed that performs blanket CVD Al depositions from tri-isobutyl-aluminum [62]. The typical deposition conditions of 150–600 mT and $\leq 250^\circ\text{C}$ yielded deposition rates of ≤ 20 nm/m and resistivities of $2.8 \pm 0.2 \mu\Omega\text{-cm}$ [63]. The films were alloyed with up to 0.37 wt.% Cu by diffusion from sputtered overlayers or underlayers consisting of Cu or AlCu alloys [64]. Features 0.5 μm wide and having an aspect ratio of 2 were fully filled using 0.3 μm of Al on a 0.1- μm -thick PVD TiN nucleation layer. It is interesting to note that features 0.75 μm wide were filled by the same process, indicating enhanced filling of wider features that would facilitate RIE patterning or planarization by CMP. The achievement of uniform filling required the formation of a continuous seed layer. Since conventional PVD TiN was used, reduction of the TiN thickness to 300 Å produced poor Al filling. It is likely that enhanced scalability would result from coupling this process with CVD Ti and TiN.

Selective CVD-Al has also been demonstrated, though on a laboratory scale. Dimethyl-aluminum-hydride

(DMAH), dimethyl-ethylamine alane (DMEAA), and tri-isobutyl-aluminum have recently been evaluated [65–67]. The DMAH process appears to be closest to application in an integrated process. Vias of 0.45 μm diameter in oxide having an aspect ratio of 2 were selectively filled with undoped Al. Nucleation was provided by exposed Al from an underlying wire. Selectivity was enhanced by using a BCl_3 RIE preclean to remove native Al oxide, with the best results obtained using 0.37 W/cm² for 15 minutes.

CVD Cu has also attracted attention because of the previously mentioned scaling advantages conferred by Cu and the fact that no filling technique has yet been established as a standard for IC manufacturing. There has been extensive work in laboratory tools within IBM on organometallic precursors for blanket CVD Cu filling. For instance, trialkylphosphine(cyclopentadienyl) copper(I) complex has been used to deposit blanket Cu [68]. Since the room-temperature vapor pressure of such sources is only 1–2 mT, a relatively large flow rate (75 SCCM) was required to ensure that deposition rates depended on substrate temperature instead of mass transport. Typical deposition pressures were 5–50 mT. The process yielded useful depositions containing <1 at.% C at substrate temperatures of 150–210°C. Below 150°C, the deposition rate was <100 Å/min, while films deposited above 220°C contained large amounts of C. PVD Cr and Cu seed layers were used to enhance the nucleation of the CVD Cu. Since the deposition resulted from surface-catalyzed decomposition of the precursor, it was easily poisoned by organophosphine reaction by-products. Thus, frequent cleaning of reactor surfaces and recharging of precursor were required in order to maintain an acceptable deposition rate. A 1.5- μm -thick film was shown to conformally fill a trench measuring 2.0 μm deep and 0.7 μm wide (aspect ratio of about 3), and exhibited overburden surface roughness of 2000–3000 Å. Smoother films could be produced by using higher precursor flow rates and substrate temperatures, though at the expense of conformality.

More recently, a 1,5-cyclooctadiene copper(I) hexa-fluoro-acetylacetonate (COD-Cu-hfac) process has been demonstrated [69]. The typical flow rates used were 30–50 SCCM of precursor and 28 SCCM of He carrier gas, resulting in a process pressure of ~ 70 mT. The process provided acceptable deposition rates, 100–400 Å/min, and produced relatively pure, smooth Cu films having a low resistivity (2.0 $\mu\Omega\text{-cm}$). Blanket deposition was always observed above 200°C, though selective deposition on sputter-cleaned metal liners was obtained at lower temperatures and low COD-Cu-hfac flow rates. Conformal coverage of trenches having an aspect ratio of 1.5 was demonstrated using a sputter-cleaned 300-Å-thick PVD Ta liner.

Despite its attractive attributes, CVD of Al or Cu has not yet been adopted in chip manufacturing. As mentioned previously, the need for high-aspect-ratio filling of high-conductivity metals for damascene applications is recent. Moreover, it is desirable to extent PVD techniques as far as possible before retooling existing fabricators. Further, both Al and Cu source gases are relatively expensive and may remain so until they are manufactured in greater quantities.

Concluding remarks

The interconnects for current IBM CMOS products are formed using a mixture of damascene and cloisonné processes. Maintaining redundant patterning and deposition processes increases product fabrication costs. Cloisonné processes require more complex coadjustment of unit processes, and are less easily extendible to the formation of low-cost, aggressively scaled monolithic studs/wires than damascene processes. The *dual-damascene* process is a comparatively simple and cost-effective method for forming such advanced interconnects.

Dual-damascene Al-based and Cu-based interconnects have been developed recently. Their successful migration from development to manufacturing will require robust metal filling and CMP processes. In the near term, high-temperature PVD and Al CMP can be used to form Al-based wiring. In the longer term, more flexible, lower-temperature techniques will be required for depositing Cu as well as Al, since Cu provides scaling and planarization advantages. Ionized PVD is compatible with current manufacturing equipment, though CVD Al and Cu processes are options for the future.

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Thomas J. Licata *Materials Research Corporation, 200 Route 303N, Congers, New York 10920 (licata_tom@ny.mrc.sony.com).* Dr. Licata is Director of Process Science at the Materials Research Corporation. Prior to June 1995, while this paper was in preparation, he was an advisory engineer at the Semiconductor Research and Development Center of the Hopewell Junction, New York facility of the IBM Microelectronics Division. After joining IBM in late 1990, he worked on the development of novel interconnects and PVD-based materials and processes, and on the evaluation and selection of metal process tools for the IBM-Siemens-Toshiba 256Mb, 64Mb shrink, and 64Mb DRAMs. He obtained his B.A. in chemical physics from Columbia College in 1983, and his M.S. and Ph.D. in materials science from Columbia University in 1985 and 1990, respectively. His work at Columbia University included the development of novel thermal and photon-activated processes for compound semiconductors. He has published twenty papers on aspects of materials processing, and has been issued three patents. For the past two years, Dr. Licata has chaired the Thin Films and Interconnects session at the International Conference on Metallurgical Coatings and Thin Films.

Evan G. Colgan *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (COLGANE at YKTVMV, colgane@watson.ibm.com).* Dr. Colgan is a research staff member at the Thomas J. Watson Research Center, and manages the Thin-Film Transistor group in the Flat Panel Display Technologies Department. He joined the Research Division in 1995. Previously, while this paper was developed, he was an advisory engineer at the Semiconductor Research and Development Center in Hopewell Junction, New York. While at the Development Center, since joining IBM in 1987, Dr. Colgan worked on aspects of metal silicide formation, selective chemical vapor deposition of tungsten, diffusion barriers, Al(Cu) microstructure evolution, and integration of both Cu- and Al-based metallizations. He received his B.S. degree in applied physics from the California Institute of Technology in 1982 and his Ph.D. in materials science and engineering from Cornell University in 1987. His thesis work involved the formation of aluminides from thin-film couples. Dr. Colgan has published over fifty papers and has been issued four patents; he is a member of the MRS, IEEE, APS, Böhmische Physical Society, and Sigma Xi.

James M. E. Harper *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (HARPERJ at YKTVMV, harperj@watson.ibm.com).* Dr. Harper is a research staff member at the Thomas J. Watson Research Center, and manages the Thin-Film Metallurgy and Interconnections group in the Silicon Technology Department. Since joining IBM in 1975, he has developed quantitative low-energy ion beam techniques for modifying thin-film properties, and has applied rapid evaluation methods to thin-film reactions. He received a B.A. in physics from Harvard University in 1968, taught physics at the U.S. Coast Guard Academy, and received a Ph.D. in applied physics from Stanford University in 1975. Dr. Harper is a co-author of four book chapters, more than one hundred technical papers, and twenty patents in low-temperature physics and materials processing. He has been active in the American Vacuum Society as a Director, Thin-Film Division Chairman, Short Course Instructor, and member of the Editorial Board of the *Journal of Vacuum Science and Technology*. Dr. Harper has also served the Materials Research Society as a symposium organizer, as a Program Co-Chair of the 1994 Spring Meeting, and as a member of MRS Task Forces on Manufacturing and on Meeting Quality Improvement. He is currently a Councillor of the MRS.

Stephen E. Luce *IBM Microelectronics Division, Burlington facility, Essex Junction, Vermont 05452 (SLUCE at BTVMOFS).* Mr. Luce is a senior engineer at the IBM Burlington facility. Since joining IBM in 1978, he has developed and integrated process modules for micron- and half-micron-scale multilevel interconnects, and has applied them in a variety of CMOS products. He received his B.S. degree in physics from the University of Vermont in 1976. Mr. Luce has coauthored twelve papers on unit processes and their integration for multilevel metallization of CMOS products; he has been issued eight patents.